Product Specification

80km 100GBASE-ZR4 QSFP28 Optical Transceiver Module

PRODUCT FEATURES

- QSFP28 MSA compliant

- Hot pluggable 38 pin electrical interface

- 4 LAN-WDM lanes MUX/DEMUX design

- 4x25G electrical interface

- Maximum power consumption 6.5W

- LC duplex connector

- Supports 103.125Gb/s aggregate bit rate

- Up to 80km transmission on single mode fiber

- Operating case temperature: 0℃ to 70℃

- Single 3.3V power supply

- RoHS 2.0 compliant

APPLICATIONS

- 100GBASE-ZR4 100G Ethernet

- Telecom networking

DESCRIPTIONS

Conneu's 100GQSFP28-ZR4-80-1310 is designed for 80km optical communication applications. This module contains 4-lane optical transmitter, 4-lane optical receiver and module management block including 2 wire serial inter-face. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector. A block diagram is shown in Figure 1.
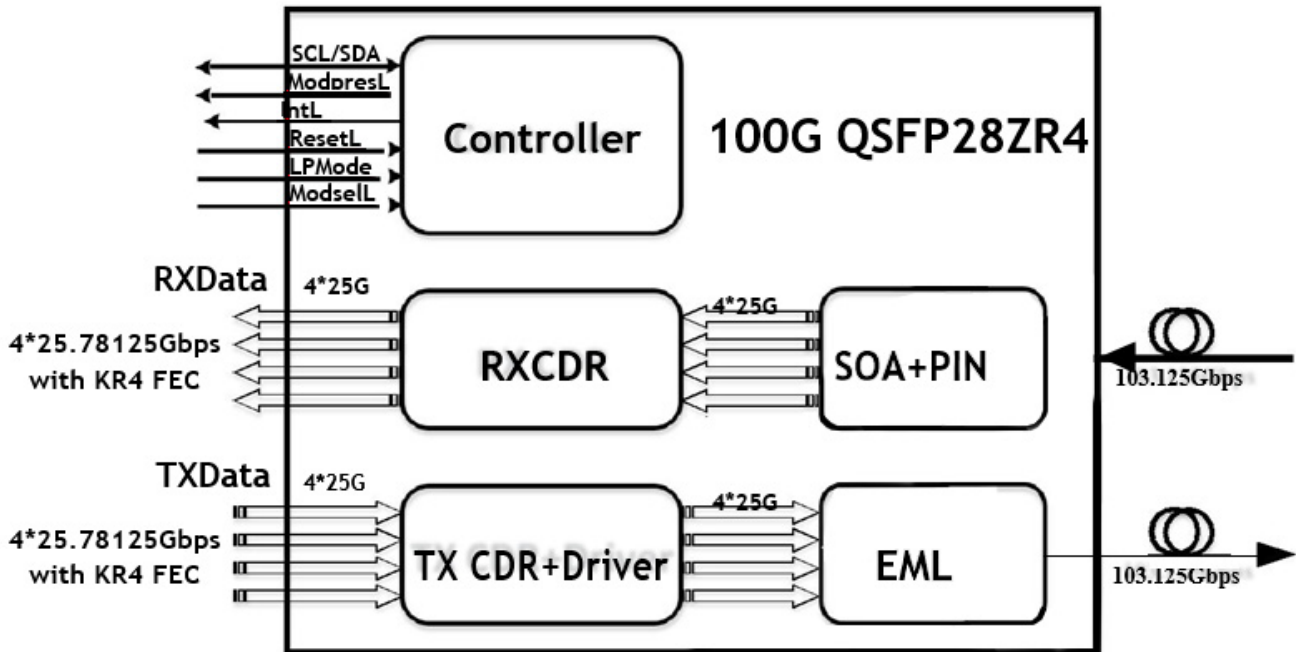
Transceiver Block Diagrams

Figure 1. Transceiver Block Diagram

ModSelL:

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the Mod-SelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the Mod-SelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL :

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the mini-mum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indi-cates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.